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Applicant: Ralf M. Schmitt et al.

## Information Disclosure Statement by Applicant

(Use several sheets if necessary)

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## U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
	A	5,644,498	7/1/97	Joly et al.	716	2	
	B	5,963,729	10/5/99	Aji et al.	716	5	
	C	6,289,412	9/11/01	Yuan et al.	703	14	
	D	5,778,216	7/7/98	Venkatesh	713	503	
	E	6,263,478	7/17/01	Hahn et al.	716	10	
	F	5,974,245	10/26/99	Li et al.	716	10	
	G	5,581,473	12/3/96	Rusu et al.	716	6	
	H	6,289,498	9/11/01	Dupenloup	716	18	
	I	5,864,487	01/1999	Merryman	716	6	
	J	5,917,729	06/1999	Naganuma	716	10	
	K	6,053,950	04/2000	Shinagawa	716	2	
	L	6,205,572	03/2001	Dupenloup	716	5	
	M	6,260,182	07/2001	Mohan	716	12	
	N	6,442,740	8/27/02	Kanamoto	716	6	
	O	5,864,487	1/26/99	Merryman			
	P	5,917,729	6/29/99	Naganuma			
	Q	6,053,950	4/25/00	Shinagawa			
	R	6,205,572	3/20/01	Dupenloup			
	S	6,260,182	7/10/01	Mohan			
	T	6,442,740	8/27/02	Kanamoto			

## Foreign Documents

Translation

Init.		Document No.	Date	Country	Class	Subclass	Yes	No
	U	WO 95/34036	12/14/95	WO				

## Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

	V	R.B. Mueller et al., "Parallel Switch-Level Simulation for VLSI", IEEE, 1991, pp. 324-328
	W	Scot Boon et al., "High Performance Clock Distribution for CMOS Asics", IEEE 1989, pp. 15.4.1 - 15.4.5
	X	H. Fair et al., "XP-000862228 SP 25.2: Clocking Design and Analysis for a 600MHz Alpha Microprocessor", IEEE International Solid-State Circuits Conference, 1998, pp. 389-399 & 473
	Y	International Search Report, PCT/US 02/32937, International filing date October 15, 2002, date Search Report mailed January 28, 2004.

Examiner

Date Considered

4-24-2004

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.